Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.028 X .028”**

**.040”**

**.040”**

**(Side View)**

**CHIP BACK IS CATHODE**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .028” X .028”**

**Backside Potential: Cathode**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 10/21/21**

**MFG: SUSSEX THICKNESS .010” P/N: 1N4001**

**DG 10.1.2**

#### Rev B, 7/19/02